CRC | Payload | Seq.#

30 bits

35 bits

17 bits

12 bits

77 58 17 0

Single-Hit Packet (excluding inversion bits)

FIG. 1

Single-fllt Packet (excluding 11 inversion bits)

47 bits

30 bits

CRC (Payload & Seq. #)

PAYLOAD

77   46   206   204   0

FIG. 2

202

206

302 Payload - 47 bits

47 bits

304 CRC 30 bit CRC (P)

308

310 30 bit CRC (t)

47 bits

306 Sequence # 12 bits

12 bit Seq #

CRC 30 bit CRC (s)

312 Encoder Inversion bits

47 bits

77 bits

88 bit Packet (one flit)

To Serial Link

FIG. 3

FIG. 4A

402

Code Word 10 ... Code Word 1 ... Code Word 0

87 · · · D7 ... D1 I

15 · · · D7 ... D1 I 8 7 · · · D7 ... D1 I 0 :Bits
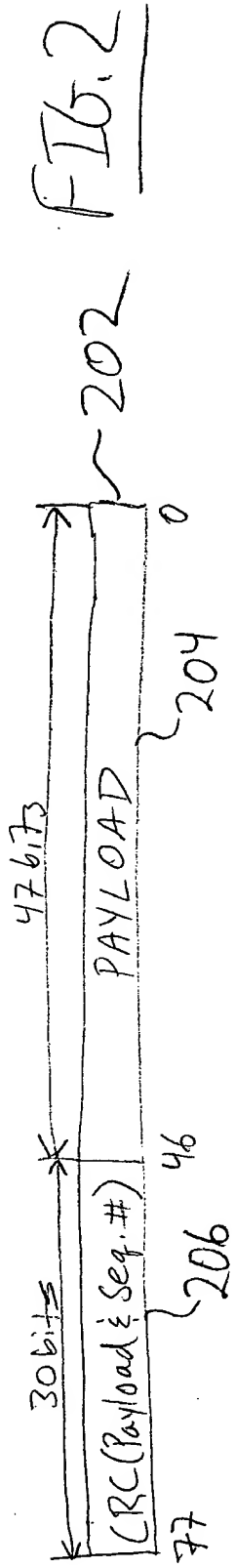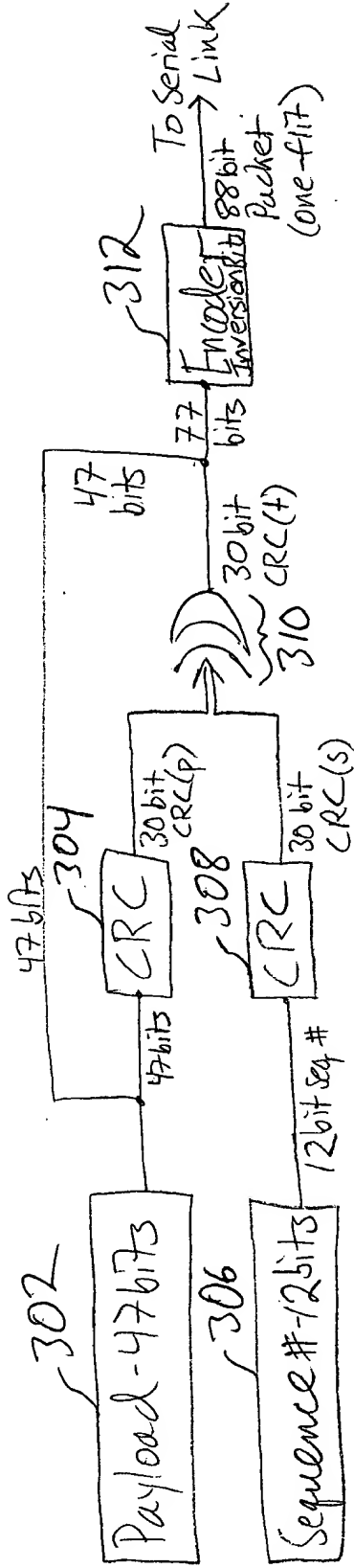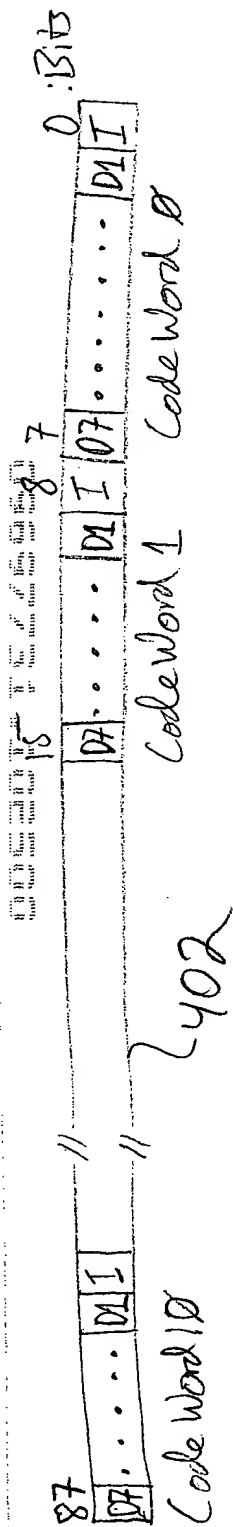
FIG.4B

Receiver Node

Receive encoded 88-bit packet ~404

Strip out invert bits (77 bits left) ~406

Input into CRC generator ~408

CRC generator computes 30-bit CRC value based on 47-bit data ~410

Fix up encoded data based on invert bits ~412

Check whether error is from sequence # or transmission error ~414

DONE

FIG. 4C

416 | Inv (11) | CRC (30) | PAYLOAD (47) bits | 416

↓ 47

418 — CRC_XOR TREE

↓ 30
CRC_XOR

420 — DECODE COMPENSATION

↓ 30
CRC_INV_XOR

422 — decode CRC

decoded CRC

30 47

30 47

424

[11:0]
CRC_OUT

428 — SEQ XOR — 30 — 11:0 unused

426 — Expected SN — SEQ XOR

430 — = — accept_packet

[29:12]

[29:12]

432 — [29:12] — != — transmission error